REMARKS

The Applicants have filed the present Response in reply to the outstanding Official Action of October 6, 2004, and the Applicants believe the Response to be fully responsive to the Official Action for reasons set forth below in greater detail.

At the onset the Applicants would like to thank the Examiner for indicating that Claims 6 and 7 have allowable subject matter and would be allowed if rewritten in independent format including all of the limitations of the rejected base claim and all intervening claims. However, since the Applicants believe that all of the claims are allowable over the cited prior art based upon the following analysis, the Applicants respectfully request the Examiner to reconsider the present application in light of the present response.

Additionally, the Applicants would like to note that dependant Claims 9-11 have been added to the application for examination. New Claims 9-11 are dependant on Claim 1 and do not add any new matter. Specific support therefore can be found on page 15 of the specification. Claims 9-11 are patentably distinct from the cited references in the outstanding Official Action for at least the reasons set forth herein.

In the Outstanding Official Action, the Examiner rejected Claims 1-5 and 8 under 35 U.S.C § 103(a) as being unpatentable over Schwalke U.S. Patent No. 5,932,919, in view of Takashima et al. U.S. Patent No. 5,953,246 (hereinafter "Takashima") in further view of Yamazaki U.S. Patent No. 6,573,575 and in further view of Noble et al. U.S. Patent No. 6,573,169 (hereinafter "Noble").

Specifically, the Examiner contends that Takashima discloses an n-channel transistor with a p-type gate and that such a gate allows the transistor to have a high threshold voltage value. In addition, the Examiner asserts that Yamazaki discloses that it is well known in the art that memory transistors have a higher threshold voltage than that of the peripheral circuitry in order to reduce subthreshold leakage current with the memory transistors, and to realize high speed operation via a lower on resistance within the peripheral circuitry. Thus, the Examiner concluded that in view of Yamazaki and Takashima that it would be obvious to use an n-channel transistor with a p-type gate.

The Applicants respectfully disagree with the Examiner's rejection and traverses the rejection with at least the following analysis.

Takashima teaches that it is desirable to have the gate type different from the channel type, for example, use a p-type gate with an n-channel transistor, and an n-type gate with a p-channel transistor, so as to increase the threshold voltage. This is achieved by the difference in working function between the gate and the channel. Yamazaki teaches that it is desirous to have transistors with high thresholds for memory cells.

However, Yamazaki teaches away from using a p-type gate with an n-channel transistor. First, **the subthreshold leakage current increases instead of being reduced**. See Col 4, lines 21-35 ("In the FET having the gate electrode formed by using the p+ poly silicon film...In this case, the subthreshold factor of the FET lowers, with the result that controllability of the source-drain current by the gate voltage is deteriorated, and the subthreshold leakage current increases.).

Additionally, boron included in the p+ polysilicon film is liable to be captured into the SiO_2 of the gate oxide film in a heat treatment step, in comparison with phosphorus included in the n+ polysilicon film. Therefore, the threshold voltage of the FET changes, and the insulating performance of the gate insulating film lowers, ***so that reliability drops***. See Col 4, lines 36-41. Reliability for memory transistors is extremely important and therefore any structure that is known to cause a decrease in reliability would not be used for memory transistors, thus this teaches away from using this particular structural formation.

Moreover, when the gate electrode of the memory cell FET is formed by using the p-type polysilcon film and the gate electrode of the peripheral circuit FET is formed with a n-type polysilicon film, the number of fabrication steps increases as it is not possible to use a common interconnection material for connecting the respective gate electrodes. Therefore, for the cited reasons Yamazaki teaches away from using a p-gate with an n-channel transistor as the memory cell transistor. In fact, Yamazaki teaches an N-type gate with an n-channel transistor.

While the claimed invention uses a p-type gate with an n-channel transistor, the claimed invention overcomes the above-cited problems. Specifically, the invention uses a P^+ type gate with a NMOS transistor in which ***the difference in Fermi level between the gate electrode and the P-type substrate is small.*** Since the gate electrode of the P^+ gate NMOS is not depleted, the concentration of boron introduced into the gate can be selected to be relatively small, taking the boron penetration into consideration.

The P^+ gate NMOS is formed in a p-well as a substrate. By selecting a p-type substrate and controlling the Fermi level of the p-type gate (i.e. lowest Fermi level) , the inventor was able to overcome the problems of using a p-type gate with an n-channel

transistor as the memory transistor. Furthermore, by using a p^+ gate NMOS transistor in the memory cell as claimed, it is possible to reduce the concentration of the p type impurity that is injected into the channel in order to increase Vth. As a result, it is possible to decrease the junction field between the substrate and a low-concentration n type diffusion layer of the source/drain (SD). Therefore, it is possible to reduce pn junction leak current which is a predominant factor of leak current of the memory cell meaning that the refresh cycle can be extended.

The transistor as claimed, reduces the dosage of boron as compared with the n^+ gate NMOS. As a result, it is possible to remarkably reduce the junction field between the n-layer of the memory cell and the p-well and to reduce the pn junction leak current. Additionally, the influence of boron penetration upon the p-well is small as compared with the influence of boron penetration upon the n-well.

Additionally, Yamazaki does not disclose that memory transistors have a higher threshold voltage than that of the peripheral circuitry. The reference solely teaches that it is desired to have a high threshold voltage in the memory section. The reference does not teach any comparison with the threshold value of the peripheral circuitry. Further, the reference does not appear to teach that there is a lower resistance within the peripheral circuitry as a result of using a p-type gate with an n-type channel.

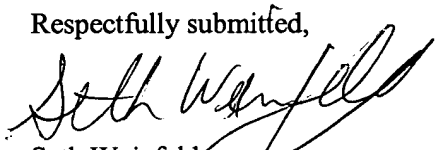
Accordingly, there is no motivation to combine the references and no teaching of "a P type polysilicon having a lowest Fermi level is disposed on a first N-type surface channel MOS transistor" as specifically claimed in Claim 1 or "a P+ gate NMOS containing a P type impurity alone which is disposed in a memory cell" as claimed in Claim 8.

Claims 2-5 are patentably distinct for the same reasons as set forth above.

For all the foregoing reasons, the Applicants respectfully requests the Examiner to withdraw the rejections of Claims 1-5, and 8 pursuant to 35 U.S.C. § 103(a). Additionally, the Applicants submit that new Claims 9-11 are patentably distinct from all of the cited references.

In conclusion, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicant respectfully requests that the Examiner call the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,



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